IN THE DRAWINGS:

The attached sheets of drawings include Figures 1-4 that have been redrawn to provide more legible text in each box. No other changes have been made to Figures 1-4. Replacement Sheet 1 includes Figures 1-2 and Replacement Sheet 2 includes Figures 3-4.

Attachment: Replacement Sheets 1-2

REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-21 in the application. The Applicant has amended Claims 1-2, 4-16 and 18-21. No claims have been amended or canceled. Accordingly, Claims 1-21 are currently pending in the application.

I. Formal Matters and Objections

The Examiner has objected to the drawings asserting that the labels inside the boxes of the figures cannot be legibly scanned or copied. In response, the Applicant submits replacement figures with more reproducible text. Accordingly, the Applicant respectfully requests the Examiner to withdraw the objection to the figures.

Claims 1-21 have also been objected to due to informalities. In response, the Applicant has corrected these noted informalities as suggested by the Examiner. Accordingly, the Applicant respectfully requests the Examiner to withdraw the objection to Claims 1-21 and allow issuance thereof.

II. Rejection of Claims 1-6, 8-13 and 15-20 under 35 U.S.C. §103

The Examiner has rejected Claims 1-6, 8-13 and 15-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,532,579 to Sato, *et al.*, in view of U.S. Patent No. 6,681,354 to Gupta. The Applicant respectfully disagrees.

Sato is directed to adding a custom self-examining test circuit to a semiconductor integrated circuit (IC). (*See* column 1, lines 8-14 and lines 45-48.) Sato does not teach or suggest, however, an IC including a plurality of interchangeable hard macrocells as recited in independent Claims 1, 8 and 15. Instead, Sato teaches a semiconductor chip with circuit blocks that are each prepared for a single function (*i.e.*, a CPU, a DSP, a DRAM, *etc.*). Sato provides not teaching or suggestion that the circuit blocks are interchangeable. (*See* column 12, lines 47-57 and Figures 12 and 15.)

As recognized by the Examiner, Sato also does not teach or suggest a programmable logic block. (*See* Examiner's Action , page 5.) To cure this deficiency of Sato, the Examiner cites Gupta. Gupta is directed to system-on-a-chip (SoC) devices that include an embedded field programmable gate array (FPGA) circuit that performs built-in self-test (BIST) functions. (*See* column 1, lines 8-12.) Gupta discloses a SoC device having components that are each configured for a particular function. (*See* column 4, lines 18-27, lines 40-48 and Figure 1.) Gupta does not teach or suggest a plurality of interchangeable hard macrocells as recited in independent Claims 1, 8 and 15. Accordingly, Gupta does not cure the above discussed deficiency of Sato.

Thus, the cited combination of Sato and Gupta, individually or in combination, fails to teach or suggest each element of independent Claims 1, 8 and 15 and Claims dependent thereon. Accordingly, the cited combination of Sato and Gupta do not provide a *prima facie* case of obviousness of Claims 1-6, 8-13 and 15-20 and do not render Claims 1-6, 8-13 and 15-20 unpatentable. Therefore, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 1-6, 8-13 and 15-20 and allow issuance thereof.

Moreover, one skilled in the art would not be motivated to combine Sato and Gupta. On the contrary, Sato is directed to providing an IC having a self-examining test circuit that can be configured without an increase in chip size. (*See* column 1, lines 45-47.) Accordingly, Sato uses programmable cells in between circuit blocks. Gupta, on the other hand, teaches an embedded FPGA that can be used for testing other embedded circuit components of an integrated processing system. (*See* Abstract.) Thus, Gupta teaches an embedded FPGA that is configured to perform BIST (*see* column 1, line 66 to column 2, line 4) while Sato teaches against such an embedded FPGA by employing programmable logic cells in free space to reduce chip size (*see* column 2, lines 20-31).

III. Rejection of Claims 7, 14 and 21 under 35 U.S.C. §103

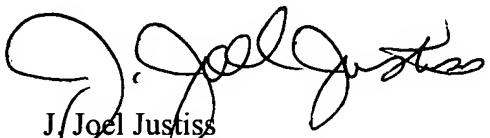
The Examiner has rejected Claims 7, 14 and 21 under 35 U.S.C. §103(a) as being unpatentable over Sato and Gupta in further view of U.S. Patent No. 5,638,382 to Krick, *et al.* The Applicant respectfully disagrees. As argued above, the cited combination of Sato and Gupta does not teach or suggest each element of independent Claims 1, 8 and 15. Krick has not been cited to cure the deficiencies of Sato and Gupta but to teach the subject matter of dependent Claims 7, 14 and 21. Thus, the cited combination of Sato, Gupta and Krick fails to teach or suggest each element of independent Claims 1, 8 and 15 and Claims dependent thereon. Accordingly, the cited combination of Sato, Gupta and Krick does not provide a *prima facie* case of obviousness of Claims 1, 8, and 15 and Claims 7, 14 and 21 which depend thereon, respectively. Therefore, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 7, 14 and 21 and allow issuance thereof.

IV. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-21.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,



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